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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, May 2013
(2008 Scheme)
Branch : Electronics and Communication
08.404 ELECTRONICS CIRCUITS – II (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Distinguish between stagger tuning and synchronous tuning.
2. Draw the circuit of a MOS based active load circuit.
3. Draw the electrical equivalent of a crystal and its reactance curve.
4. Give the effect of cascading on cut-off frequencies and bandwidth.
5. What is a cascode amplifier ? What are its features ?
6. List any two major differences between monostable and bistable multivibrators.
7. Explain the significance of stability in negative feedback amplifiers.
8. Explain how amplitude of oscillation in an oscillator is automatically stabilised.
9. Differentiate between RC and LC oscillators.
10. Explain any 3 non-ideal characteristics of a differential amplifier. **(10×4=40 Marks)**

PART – B

Answer **any two** questions from **each** Module. Each question carries **10** marks.

Module – I

11. Starting from the expressions for gain at resonant frequency, derive expression for bandwidth of a multistage single tuned and double tuned amplifiers.

12. For a dual-input unbalanced output differential amplifier, the component values are

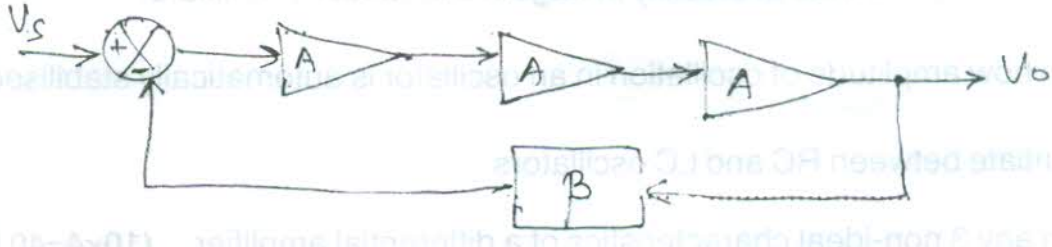
    $R_C = 2.2\,K$, $R_E = 4.7\,K$, $R_S = 50\ \Omega$, $V_{CC} = 10\ V$, $V_{EE} = 10\ V$. For the transistors $\beta = 100$ and $V_{BE} = 0.7\ V$. Determine (a) Q points (b) Voltage gain (c) CMRR.

13. For a BJT with $\beta = 100$ and $r_0 = 100\,K$, contrast the wilson mirror and the simple mirror circuits by evaluating the transfer ratio error due to finite β.

Module – II

14. A multipole amplifier having a pole at 1MHz and an openloop gain of 100 dB is to be compensated for closed loop gains as low as 20 dB by the introduction of a dominant pole. At what frequency must the new pole be placed ? Design a suitable compensator for this.

15. Draw the circuit of a CE-CB cascode. Derive expressions for its pole frequencies.

16. 

For the feedback amplifier shown, each stage has a gain of 10. The closed loop gain is 100. Determine the feedback factor. If the gain of each state increases by 10%, determine the percentage change in closed loop gain.

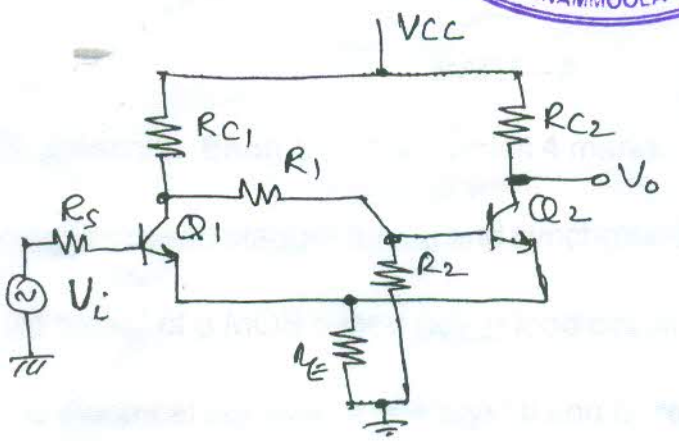
Module – III

17. For the Schmitt trigger shown, silicon transistors are used with $\beta = 20$. The circuit parameters are $V_{CC} = 12$ V, $R_S = 4$ K, $RC_1 = 3$ K, $RC_2 = 1$ K, $R_1 = 2$K, $R_2 = 8$ K and $R_E = 5$K. Calculate

    a) UTP

    b) LTP and

    c) Plot V_o for $V_i = 10 \sin \omega t$.



18. A collector coupled monostable multi using npn silicon transistors has $V_{CC} = 12$ V, $V_{BB} = 3$ V, $R_C = 2$ K, $R_1 = R_2 = R = 20$ K, $\beta = 30$, $rbb' = 200\ \Omega$, and C = 1000 pF.

    a) Calculate and plot to scale the waveform at each base and collector

    b) Find the width of the output pulse.

19. Draw the circuit of a Hartley oscillator. Derive the expression for frequency of oscillation and condition for oscillation. **(6×10=60 Marks)**